The ICFAI University – Dehradun
Faculty of Science and Technology
First Semester, 2015-2016
Course Handout

Course No.	Course Title	L	P	U
MEL 601	**HDL based Digital Design (using VHDL)**	**3**	**2**	**4**

Scope and Objective of the Course:

To provide basic knowledge of digital circuits and to write their HDL codes. After going through this course the students will be able to design HDL codes for various arithmetic operations. Further they will be able to design logic devices and systems by HDL codes.

Text book(s)	
T1	J. Bhasker, *A VHDL Primer*, Third Edition, PH/Pearson, 1999
Reference Book (s)	
R1	Z. Navabi, *VHDL : Analysis and Modeling of Digital Systems,* Second Edition, MH, 1998..
R2	P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.
R3	Z. Navabi, *VHDL : Modular Design and Synthesis of Cores and Syestems,* Third Edition, MH, 2008..

Lecture-wise Plan

Lecture No.	Learning Objectives	Topics to be covered	Reference No.(s)
1 – 4	Introduction to VHDL	VHDL description, History, Capabilities, Hardware abstraction, Basic Terminology, Model analysis and simulation	T1
5 – 10	Basic Language Elements	Identifiers, Data Objects, Data Types, Operators	T1
10 – 15	Behavioral Modeling	Entity Declaration, Architecture Body, Process statement, Variable assignment, Signal assignment, Wait, If, Case, Null, Loop, Exit, Next, and Assertion statements, Postponed Processes	T1
15 – 20	Data Flow Modeling	Concurrent signal assignment, Concurrent vs. Sequential signal, Multiple drivers, Conditional signal assignment, Selected signal assignment, Block and Concurrent assertion statements, Unaffected value, value of a signal	T1

21 – 23	Structural Modeling	Component Declaration, Components Instantiation, Examples	T1
24 – 26	Generic and Configurations	Generics, Configuration specification and declarations, Default rules, Conversion functions, Direct Instantiation	T1
27-29	Subprograms and Overloading	Subprograms and overloading, operator overloading, Signature and default values for parameters	T1
30-32	Packages and Libraries	Package declaration, Package Body, Design file and libraries, Order of Analysis, Implicit and Explicit visibility	T1
33-35	Advanced Features	Entity and Generate Statements, Aliases, Guarded Signals, Attributes	T1
36-40	Model Simulations and Hardware Modeling Examples	Simulations, Writing a Test bench, Dumping results into a text file, Reading vectors from a text file, State Machine Modeling, Moore and Melay FSM modeling, Generic priority encoder and Binary multiplier and other examples	T1

HDL Based Digital Design (List of Laboratory Experiments)

Objective of this lab is to provide experimental exposure of designing and simulation using HDL software tools.

1. Design and simulation of Logic gates.
2. Design and simulation of XOR gate using NAND gate only.
3. Design and simulation of comparator.
4. Design and simulation of Full Adder and Full Subtractor.
5. Design and simulation of Multiplexer and De-multiplexer.
6. Design and simulation of Encoder and Decoder.
7. Design and simulation of Flip-Flops.
8. Design and simulation of UP-DOWN counter/Decade counter.
9. Design and simulation of different Shift Registers.
10. Design and simulation of Binary Multiplier.
11. Design and simulation of Floating Point Arithmetic.
12. Individual Mini-Project.

The ICFAI University – Dehradun
Faculty of Science and Technology
First Semester, 2015-2016
Course Handout

Course No.	Course Title	L	P	U
MEL 601	**HDL based Digital Design (using Verilog HDL)**	**3**	**2**	**4**

Scope and Objective of the Course:

To provide basic knowledge of digital circuits and to write their HDL codes. After going through this course the students will be able to design HDL codes for various arithmetic operations. Further they will be able to design logic devices and systems by HDL codes.

Text book(s)	
T1	Samir Palnitkar, Verilog HDL A Guide to Digital Design and Synthesis, Pearson India, 2nd Edition, 2003.
T2	Peter J. Ashenden, Digital Design, An Embedded System Approach using Verilog, Elsevier, 2008.
T3	Stephen Borwn, Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, Tata McGraw Hill, 2002.
Reference Book (s)	
R1	Peter Minns, Ian Elliott, FSM-based Digital Design using Verilog HDL, John Wiley & Sons Ltd, England, 2008.
R2	J. Bhasker, Verilog HDL Primer 3rd Edition, Pearson Education, 2005.
R3	Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, Fourth Edition, Springer, 2014.
R4	M. Morris Mano, Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, Fifth Edition, Pearson, 2013.

Lecture-wise Plan

Lecture No.	Learning Objectives	Topics to be covered	Reference No.(s)
1 – 8	Introduction to Verilog HDL	Basic Concepts: Lexical conventions, Data types, System tasks and compiler directives. Modules and ports: Modules, Ports, Hierarchical Names. Gate-Level Modeling: Gate types, Gate delays.	T1, T2, T3
9 – 13	Dataflow Modeling	Continuous Assignments, Delays, Expressions, operators, and Operands, Operator types and related examples.	T1, T2, T3
14 – 18	Behavioral Modeling	Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops,	T1, T2, T3

		Sequential and Parallel blocks, Generate Blocks, related examples	
19 – 26	Task and Functions, useful Modeling Techniques, Timing and Delays	Differences between Tasks and Functions, Tasks, Functions. Procedural Continuous Assignments, Overriding Parameters, Conditional Compilation and Execution, Time scales, Useful System Tasks. Types of Delay Models, Path Delay Modeling, Timing Checks, Delay Back-Annotation.	T1, T2, T3
27 – 34	Switch-Level Modeling and User-Defined Primitives	Switch-Modeling Elements, Related examples. UDP basics, Combinational UDPs, Sequential UDPs, UDP Table shorthand symbols, guidelines for UDP Design.	T1, T2, T3
35 – 42	Writing Testbenches, System Verilog Simulation and Synthesis	Basics of testbenches, testbench structure, constrained random stimulus generation, object-oriented programming, Assertion-based verification. System Verilog Simulation: Event-Driven Simulation, System Verilog simulation, Races, Delay models, Simulator tools. System Verilog Synthesis: RTL Synthesis, Constraints, Synthesis for FPGAs, Behavioral Synthesis, Verifying Synthesis Results.	T1, T2, T3

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